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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/768,668

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EXAMINER

SITTA, GRANT

ART UNIT

PAPER NUMBER

2629

MAIL DATE

DELIVERY MODE

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/768,668	Applicant(s) SAEKI, YUTAKA	
	Examiner GRANT D. SITTA	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 September 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3, 6, 7 and 25-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 6, 7 and 25-29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 May 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 1, 2, 13, 14, 25-27, 29-30 rejected under 35 U.S.C. 102(e) as being anticipated by DeCaro et al (6,965,360) hereinafter, DeCaro.

3. In regards to claim 1, DeCaro teaches a current-drive apparatus for a display panel (abstract, “visual displays” fig. 1 (100)), comprising: a plurality of current-drive circuits (fig. 7 and 11 (710, 720, etc)), each of said plurality of current-drive circuits section including first (fig. 7 input to 200 from 750 in 710) and second (fig. 7 (200) output 716 to 200 of 720) terminals a reference resistor connected between said first and second terminals (fig. 2 (240 and 246)) and a reference current generation circuit (fig. 2 (200) “balancing circuit”) responding to a voltage generated based on the reference resistor to produce at least one internal reference current (col. 6, lines 3-15) a current source (fig. 7 and 11 (750)), said current source and said plurality of current-drive circuits being connected such that a current flowing through said current source becomes substantially equal to a current flowing through said reference resistor

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of each (col. 15, lines 18-20) of said current-drive circuits (col. 14-15, lines 64-28), wherein a current flowing through said reference resistor in a first one of said current-drive circuits flows through said reference resistor in a second one of said current-drive circuits (fig. 7 and 11 (750) and I_{ref})), and

wherein said current drive circuits are coupled in series (fig. 7 710, 720 and 730 are in series) in a manner that said first terminal of a preceding one of said current drive circuits is connected to the second terminal of a succeeding one of said current-drive circuits which is adjacent to the preceding one of said current-drive circuits (first (fig. 7 input to 200 from 750 in 710) and second (fig. 7 (200) output 716 to 200 of 720) terminal which are connected in series, while not directly connected, the first and second terminal are connected to the succeeding current drive circuit).

4. In regards to claim, 25 DeCaro teaches a current-drive system for a display panel (fig. 1 (100)), comprising: first and second power source lines (fig. 2 common electrode line and ground col. 5, lines 54-67); a plurality of current-drive ICs (fig. 7 (710-730)), each of said plurality of current-drive ICs having first and second terminals (fig 7 input and output terminals of 710-730) and having a first resistor connected between said first and second terminals (fig. 2 (240) and 242); and

a current source (fig. 2 (270)) connected to said plurality of current-drive ICs so that said ICs and said current source are connected in cascade (fig. 7 (710, 720, and

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730)) with said first and second terminals between first and second power source lines (col. 14-15, lines 64-28).

wherein said ICs are coupled in series (fig. 7 710, 720 and 730) between said first power source line and said current source in such a manner that the second terminal of a preceding one of said ICs is connected to the first terminal of a succeeding one of said ICs (fig. 7 710, 720 and 730 col. 14-15, lines 29)

5. In regards to claim 2, DeCaro teaches the current-drive apparatus according to claim 1, wherein at least one of said plurality of current-drive circuits further includes at least one current adjustment resistor (fig. 2 (240 and 242) the matched resistors compensate for current imbalance col. 6, lines 55-58) and operates so that a reference voltage generated across said reference resistor is applied across said at least one current adjustment resistor to generate said at least one internal reference current (col. 6, lines 55-58).

6. In regard to claim 26, DeCaro teaches the system as claimed in claims 25, wherein at least one of said plurality of current- drive ICs produces an internal reference voltage based on a voltage generated across said first resistor (fig. 2 (240 and 242)). Examiner notes it is inherent to have an internal reference voltage produced when an internal reference current is applied across a resistor.

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7. In regards to claim 27, DeCaro teaches the system as claimed in claims 25, wherein at least one of said plurality of current- drive ICs further includes a second resistor having a first end coupled to one end of said first resistor and having a second end coupled to the other end of said first resistor (fig. 2 (240 and 242)). Examiner notes that they are directly connected through 298 and other ends are connected through the common electrode.

8. In regards to claim 29, DeCaro teaches a current-drive apparatus according to claim 1, wherein said current-drive circuit is operable to sum up at least one internal reference current in a desired number and output a desired number of internal reference currents to a display element of said display panel (fig. 2 (260a-260e)). Examiner notes the total current is the sum of the currents through the individual components, in accordance with Kirchhoff's current law.

9. In regards to claim 30, DeCaro teaches a current drive circuit according to claim 13, wherein said current-drive circuit is operable to sum up said at least one internal reference current in a desired number and output a desired number of internal reference currents (fig. 2 (260a-260e)). Examiner notes the total current is the sum of the currents through the individual components, in accordance with Kirchhoff's current law.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 3, 6, 7, 15, 16 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeCaro, in view of Yatabe et. al (US 6,188,395) hereinafter, Yatabe.

13. In regards to claim 3, DeCaro discloses the limitations of the current-drive apparatus of claim 1.

DeCaro differs from the claimed invention in that DeCaro does not disclose wherein said reference resistor of a current-drive circuit chosen out of said plurality of current drive circuits and located on the side of a high voltage supply is connected to said high voltage supply through a voltage adjustment resistor and said reference

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resistor of a current-drive circuit chosen out of said plurality of current-drive circuits and located on the side of a low voltage supply is connected to said current source.

However, Yatabe teaches wherein said reference resistor of a current-drive circuit chosen out of said plurality of current drive circuits and located on the side of a high voltage supply is connected to said high voltage supply through a voltage adjustment resistor and said reference resistor of a current-drive circuit chosen out of said plurality of current-drive circuits and located on the side of a low voltage supply is connected to said current source (fig. 1 VDD and R1 col. 7, lines 1-20 of Yatabe).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify DeCaro to include the use of wherein said reference resistor of a current-drive circuit chosen out of said plurality of current drive circuits and located on the side of a high voltage supply is connected to said high voltage supply through a voltage adjustment resistor and said reference resistor of a current-drive circuit chosen out of said plurality of current-drive circuits and located on the side of a low voltage supply is connected to said current source as taught by Yatabe in order to change the voltage and thus provide a reduction of voltage resistance in the circuit device which causes the production cost and power source circuit to be reduced as stated in (col. 7, lines 1-10 and col. 4, lines 45-47 of Yatabe).

14. In regards to claim 6, DeCaro discloses the limitations of the current-drive apparatus according to claim 2.

DeCaro differs from the claimed invention in that DeCaro does not disclose wherein at least one of said plurality of current-drive circuits further includes a first operational amplifier, provided as a voltage follower, for outputting a voltage appearing at a terminal of said reference resistor on the side of a high voltage supply and a plurality of second operational amplifiers, provided as a voltage follower, for outputting a voltage appearing at a terminal of said reference resistor on the side of a low voltage supply, and wherein said at least one of said plurality of current-drive circuits is configured so that an output of said first operational amplifier and an output of each of said plurality of second amplifiers are applied to both ends of each of said at least one current adjustment resistor to generate corresponding one of said at least one internal reference current

However, Yatabe teaches a system and method for wherein at least one of said plurality of current-drive circuits further includes a first operational amplifier (fig. 1 2a), provided as a voltage follower (fig. 1 (2a) voltage follower), for outputting a voltage appearing at a terminal of said reference resistor (fig. 1 R8) on the side of a high voltage supply (fig. 1 (VDD)) and a plurality of second operational amplifiers (fig. 1 (2b)), provided as a voltage follower (fig. 1 (2b) voltage follower), for outputting a voltage appearing at a terminal of said reference resistor on the side of a low voltage supply (fig. 1 VEE), and wherein said at least one of said plurality of current-drive circuits is configured so that an output of said first operational amplifier and an output of each of said plurality of second amplifiers are applied to both ends of each of said at least one current adjustment resistor to generate corresponding one of said at least one internal

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reference current ((fig. 1 R8,R9, R10 and R11 is applied to both terminals col. 7, lines 1-30 of Yatabe).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify DeCaro to include the use of wherein at least one of said plurality of current-drive circuits further includes a first operational amplifier, provided as a voltage follower, for outputting a voltage appearing at a terminal of said reference resistor on the side of a high voltage supply and a plurality of second operational amplifiers, provided as a voltage follower, for outputting a voltage appearing at a terminal of said reference resistor on the side of a low voltage supply, and wherein said at least one of said plurality of current-drive circuits is configured so that an output of said first operational amplifier and an output of each of said plurality of second amplifiers are applied to both ends of each of said at least one current adjustment resistor to generate corresponding one of said at least one internal reference current as taught by Yatabe in order to provide a means to reduce the potential difference between the two driving potentials and thus provide a reduction of voltage resistance in the circuit device which causes the production cost and power source circuit to be reduced as as stated in (col. 4, lines 25-47 of Yatabe).

15. In regards to claim 7, DeCaro as modified by Yatabe teaches the current-drive apparatus according to claim 6, wherein said at least one of said plurality of current-drive circuits further includes a reference current part (fig. 1 C5 and C6of Yatabe)) disposed between each of said of current adjustment resistor and said low voltage

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supply (fig. 1, R8,R9, R10 and R11 and VEEof Yatabe), and is configured so that an output of corresponding one of said plurality of second operational amplifiers is input to said reference current part in order to allow said corresponding one of said at least one internal reference current to flow to said low voltage supply (fig. 1 through OP4 through C4 the smoothing capacitor of Yatabe).

16. In regards to claim 28, DeCaro discloses the limitations of the system as claimed in claims 25, wherein at least one of said plurality of current- drive ICs further includes.

DeCaro differs from the claimed invention in that DeCaro does not disclose a first OP amplifier having an input coupled to a node between said first terminal and said first resistor and an output thereof; a second OP amplifier having an input coupled to a node between said second terminal and said first resistor and an output thereof; and a second resistor coupled between the outputs of said first and second OP amplifiers.

However, Yatabe teaches a system and method for a first OP amplifier having an input coupled to a node between said first terminal and said first resistor and an output thereof (fig. 1 OP1 and R8); a second OP amplifier having an input coupled to a node between said second terminal and said first resistor and an output thereof; and a second resistor coupled between the outputs of said first and second OP amplifiers (fig. 1 OP2 and R9).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify DeCaro to include the use of a first OP amplifier having an input

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coupled to a node between said first terminal and said first resistor and an output thereof; a second OP amplifier having an input coupled to a node between said second terminal and said first resistor and an output thereof; and a second resistor coupled between the outputs of said first and second OP amplifiers as taught by Yatabe in order to provide a means to reduce the potential difference between the two driving potentials and thus provide a reduction of voltage resistance in the circuit device which causes the production cost and power source circuit to be reduced as stated in (col. 4, lines 25-47 of Yatabe).

Response to Arguments

17. Applicant's arguments filed 09/02/2008 have been fully considered but they are not persuasive.

18. In response to Applicant's remarks that the prior art of record fails to teach each of the current-drive circuits includes first and second terminals with a reference resistor connected therebetween, and the first terminal of a preceding one of the current-drive circuits is connected to the second terminal of a succeeding one of the current-drive circuits. The current-drive circuits are thus connected to each other at the terminal connected to the reference resistor (Remarks, page 11 of 13). Examiner respectfully disagrees. Fig. 7 of DeCaro shows an embodiment of the balancing circuits 200 configured in a daisy chained circuit or in series. The first and second terminals of Applicant's invention would be the input and output of the respective balancing circuits

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in series. In fig. 2 DeCaro shows the schematic diagram of a balancing circuit with at least one reference resistor as shown above. Examiner notes the cited claim language does not require the reference resistor to be directly connected to the first and second terminals.

Conclusion

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GRANT D. SITTA whose telephone number is (571)270-1542. The examiner can normally be reached on M-F 9-6.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/Grant D Sitta/
Examiner, Art Unit 2629
December 2, 2008